11. F. Capasso, K. Alavi, A. Y. Cho, P. W. Foy and C. G. Bethea, International Electron Device Meeting Digest, p. 468, Washington, DC, December 5-7, 1983.
12. A. Y. Cho and J. R. Arthur, Progress in Solid State Chemistry, edited by G. Somorjai and J. O. McCaldin (Pergamon, New York, 1975), Vol. 10, p. 157.
13. A. Y. Cho, Thin Solid Film 100, 291 (1983).
14. P. A. Barnes and A. Y. Cho, Appl. Phys. Lett. 33, 651 (1978).
15. J. V. DiLorenzo, W. C. Niehaus and A. Y. Cho, J. Appl. Phys. 50, 951 (1979).
16. A. Y. Cho and P. D. Dernier, J. Appl. Phys. 49, 3328 (1978).
17. A. Y. Cho, E. Kollberg, H. Zirath, W. W. Snell, and M. V. Schneider, Elec. Lett. 18, 424 (1982).
18. H. C. Casey, Jr., A. Y. Cho, D. V. Lang, and E. H. Nicollian, J. Vac. Sci. Technol. 15, 1408 (1978).
19. R. F. C. Farrow, P. W. Sullivan, G. M. Williams, G. R. Jones, and D. C. Cameron, J. Vac. Sci. Technol. 19, 415 (1981).
20. C. W. Tu, S. R. Forrest, and W. D. Johnston, Jr., Appl. Phys. Lett. 43 569 (1983).
21. A. Y. Cho and F. K. Reinhart, Appl. Phys. Lett. 21, 355 (1972).
22. W. T. Tsang and A. Y. Cho, Appl. Phys. Lett. 32, 491 (1978).
23. A. Y. Cho and W. C. Ballamy, J. Appl. Phys. 46, 783 (1975).
24. W. T. Tsang and A. Y. Cho, Appl. Phys. Lett. 30 293 (1977).
25. K. Tabatabaie-Alavi, A. N. M. M. Choudhury, K. Alavi, J. Vlcek, N. Slater, C. G. Fonstad, and A. Y. Cho, IEEE Electron Dev. Lett. EDL-3, 379 (1982).
26. K. Y. Cheng and A. Y. Cho, J. Appl. Phys. 53, 4411 (1982).
27. Y. Kawamura, Y. Moguchi, H. Asaki, and H. Nagai, Electron Lett. 18, 91 (1982).
28. J. Massies, J. Rochette, P. Delescluse, P. Etienne, J. Chevrier and N. T. Linh, Electron. Lett. 18, 758 (1982).
29. K. Y. Cheng and A. Y. Cho, J. Appl. Phys. 53, 4411 (1982).
30. M. A. Brummell, R. J. Nicholas, J. C. Portal, K. Y. Cheng, and A. Y. Cho, J. Phys. C: Solid State Phys. 16, L579 (1983).
31. K. Alavi, H. Temkin, W. R. Wagner and A. Y. Cho, Appl. Phys. Lett. 42, 254 (1983).
32. R. J. Malik, J. R. Hayes, F. Capasso, K. Alavi, and A. Y. Cho, IEEE Electron. Dev. Lett. EDL-4, 383 (1983).
33. A. Y. Cho, J. Vac. Sci. Technol. 16, 275 (1979).
34. W. T. Tsang, F. K. Reinhart and J. A. Ditzenberger, Appl. Phys. Lett. 41, 1094 (1982).
35. M. B. Panish and S. Sumski, J. Appl. Phys. (to be published).
36. M. B. Panish and S. Sumski, Appl. Phys. Lett. (to be published).
37. A. R. Calawa, Appl. Phys. Lett. 38, 701 (1981).
38. M. B. Panish, J. Electrochem. Soc. 127, 2729 (1980).
39. H. Temkin, K. Alavi, W. R. Wagner, T. P. Pearsall, and A. Y. Cho, Appl. Phys. Lett. 42, 845 (1983).
40. R. People, K. W. Wecht, K. Alavi, and A. Y. Cho, Appl. Phys. Lett. 43, 118 (1983).
41. J. R. Arthur and J. J. LePore, J. Vac. Sci. Technol. 6, 545 (1969).
42. C. T. Foxon, B. A. Joyce and M. T. Morris, J. Cryst. Growth 49, 132 (1980).
43. F. Capasso, J. Vac. Sci. Technol. B1, 457 (1983).
44. A. Y. Cho, C. N. Dunn, R. L. Kuvas, and W. E. Schroeder, Appl. Phys. Lett. 25, 224 (1974).
45. J. P. Faurie and A. Million, J. Cryst. Growth 54, 582 (1982).

RECEIVED March 12, 1985

# 9

# Chemical and Physical Processing of Ion-Implanted Integrated Circuits

Joseph C. Plunkett

Department of Electrical Engineering, California State University, Fresno, CA 93740

A brief overview of the fundamentals of the chemical and physical processing of ion-implanted integrated circuits is presented. Although not intended as a thorough review paper in the field, a modest list of references are provided to which the reader may refer for more in-depth discussions of the topics covered. As well as an overview of the principles of ion-implantation, profile shaping as a means of improving device performance is discussed. Typical applications of ion-implantation in silicon and gallium arsenide devices are also covered. Finally, some basic clean-up processes for laboratory ion-implantation processing are provided.

Technologies for the chemical and physical processing of integrated circuits have advanced at a very rapid pace in recent years. The stringent requirements of improved electrical performance and further microminiaturization of integrated circuits have forced advancement of the state-of-the-art in fabrication technology. With the evolvement of sub-micron technology and the extension of monolithic integrated circuit technology to the microwave LSI range, ion implantation is playing an increasingly important role in the fabrication processes of solid state circuits and devices. Ion implantation has been the subject of numerous review articles and bibliographies in recent years (1-20).

The discussions in this paper provide fundamental and overview material suitable for the new researcher in the field of integrated circuit processing, as well as provides the user of ion implantation with some relevant design information and some recent applications to some new devices and materials.

In its most fundamental form, ion implantation is a process by which energetic, charged-particles or impurity atoms can be introduced into a target or substrate material. Often, these particles which are to be implanted are positive ions (singly or multiply ionized) which come from a suitable source. After the formation of the positive ions, they are accelerated by static electric fields, are focused or formed into a beam, and are passed through a mass analyzer. The mass analyzer is used to ensure that the beam is pure.

0097-6156/85/0290-0127$10.00/0
© 1985 American Chemical Society

The beam is often further manipulated by slits or quadrupole analyzers prior to its striking the target. As applied to the doping of materials, the ion beam must usually be made to form a raster scan of the target. The ion beam then bombards the target substrate material by a carefully controlled and quantified process whereupon most of the ions enter the substrate material. Upon the introduction of the ions into the target material, the material acquires new electrical or chemical properties.

A brief overview of some of the advantages and disadvantages of ion implantation processes in the doping of solid state semiconductor materials is presented below.

(1) Variety of sources--for most semiconductor applications the ions which are introduced must be electrically active. This means that for impurity doping of a substrate material the ions must occupy substitutional sites in the lattice structure.

(2) Variety of substrate material--although virtually any material can be implanted, one must choose a material for impurity doping in solid state semiconductors which can be electrically activated.

(3) Impurity concentration profiles can be shaped to certain specifications. One important aspect of ion implantation into semiconductors, in contrast to the diffusion process, is that the number of implanted atoms can be precisely controlled by the external system, rather than by the physical parameters of the target material.

(4) Ordinary photolithography or mechanical masking is used for impurity positioning in the substrate.

(5) Ion implantation is a low temperature process which will not usually disturb earlier impurity distributions which may have been placed in the material. An anneal cycle must, however, be considered in order to electrically activate the dopant atoms.

(6) Implantation is not solubility limited--often however, during the process of electrical activation a condition of equilibrium may be reached and precipitation of the excess impurities may occur.

(7) Electrical activation can be achieved at temperatures less than that required for diffusion in certain materials, although gallium arsenide requires a rather high temperature. In silicon, a nominal temperature of 600 to 800 degrees C is used.

(8) The process of ion implantation lends itself to automatic control. With the advent of microprocessors and microcomputers, such process control as profile shaping can be programmed into the control and made a routine and precise process.

### Ion Distribution and Penetration

Ion implantation is not an equilibrium process, although in the process of electrical activation, equilibrium may be achieved. The energetic ions lose their energy to the host lattice often creating damage to the bulk material. An annealing process is used to remove most of the damage and to electrically activate the ions. The loss of energy to the substrate material is brought about by two processes. One is by excitation and ionization of electrons. The other is by elastic collisions with nuclei. The results of violent collisions may be the displacement of atoms in the host lattice along the ion path setting up a chain reaction as long as the kinetic



energy is available. Although some of the damage to the material sets up an amorphous state, annealing can return the lattice to its crystalline form.

Certain critical alignments of the ion beam can cause channeling or guiding of the ions by the crystal lattice. This can cause deep anomolous penetration of the substrate if they are critically aligned along the axes of the target crystal.

In practice, the target is usually deliberately misaligned with respect to the major axes of the crystal. This misalignment angle is typically 7 to 10 degrees off-axis. This quenches the channeling effect and simulates an amorphous target.

**Theoretical Range Determination.** The LSS theory (21) is often used to calculate the theoretical range, $\bar{R}$, and total straggle $\Delta\bar{R}$. The straggle represents the statistical fluctuation of the total range. It is assumed that an amorphous target is used and that a Gaussian distribution is created. Figure 1 illustrates the depth distribution of implanted atoms in an amorphous target. In the first curve, the incident ion mass is less than the substrate atomic mass. In the second curve, the ion mass is greater than the host material atomic mass. As can be seen, the straggle is greater for the first case.

For practical solid state device doping, the mean perpendicular depth of penetration, $\bar{R}_p$, and the associated straggle, $\Delta\bar{R}_p$, are the important parameters. For critical masking control, however, transverse straggle, $\Delta\bar{R}_t$, can be important.

Figure 2 shows the reference coordinates and nomenclature of this geometry. Theoretical calculations of the projected range and straggle for various dopants and substrates have been calculated and shown in graphical form (4, 21-26). Some common dopant ions for silicon and gallium arsenide are shown in Figures 3, 4, 5, and 6.

**Theoretical Impurity Profile Calculations.** Using information provided by the preceding curves, a theoretical as-implanted concentration profile can be calculated in terms of the preceding parameters (from Stone and Plunkett (26) and references therein).

$$n(x,y) = \frac{s}{(2\pi)^{3/2}\,\Delta\bar{R}_p\,\Delta\bar{R}_t^{\,2}} \exp\left[-\left[\frac{x-\bar{R}_p}{(2)^{1/2}\,\Delta\bar{R}_p}\right]^2\right] \times \exp\left[-\left[\frac{y}{(2)^{1/2}\,\Delta\bar{R}_t}\right]^2\right] \quad (1)$$

where the coordinates are shown in Figure 2.
$n$ is the ion concentration for $s$ ions/unit surface perpendicular to the target surface in the $x$ direction.

For typical applications, the $\Delta\bar{R}_t$ parameter can be effectively eliminated by the beam scan which creates an overlap of the implanted ions over the transverse straggling range. Of course, the lateral straggling effect cannot be eliminated at the mask edges.

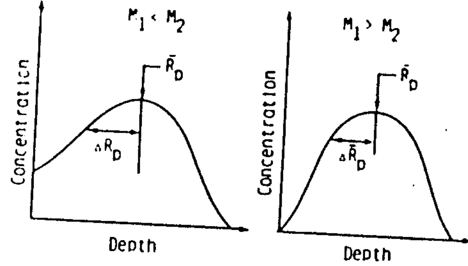


**Figure 1.** The depth distribution of implanted atoms in an amorphous target.

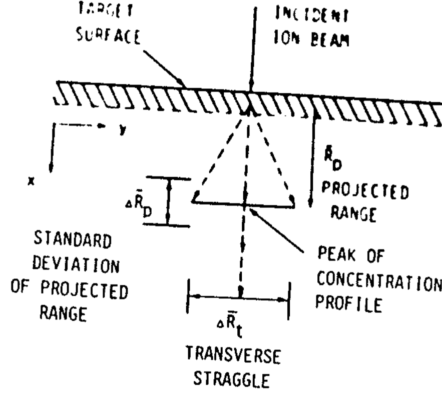


**Figure 2.** Reference coordinates for ion implantation parameters.



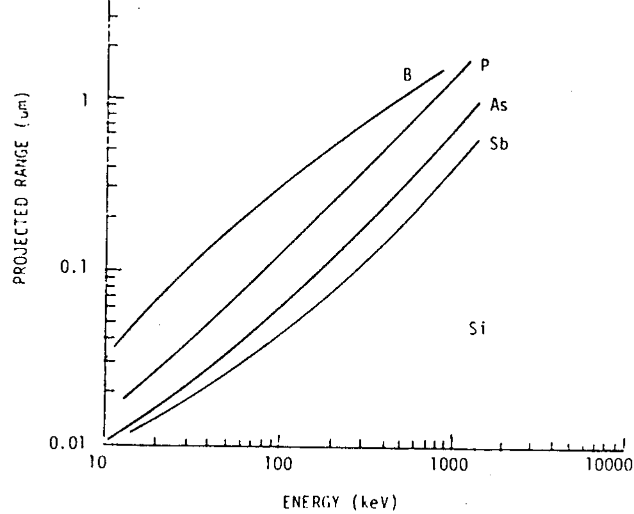


Figure 3. Theoretical calculations of the projected range of B, P, As, and Sb in silicon. (Adapted with permission from Reference 27, copyright 1983, John Wiley and Sons).

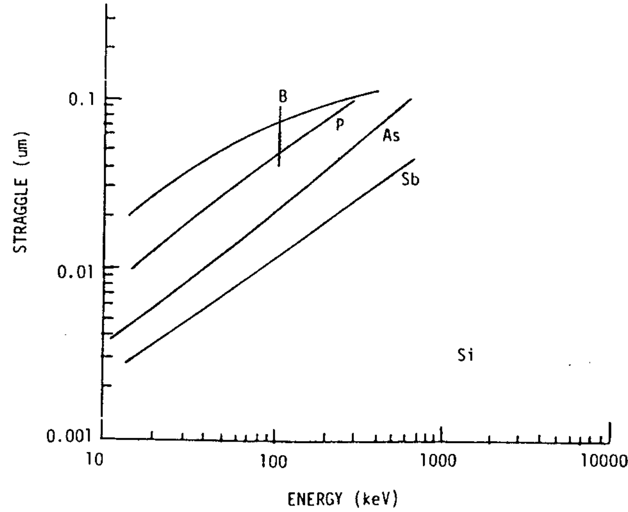


Figure 4. Theoretical calculations of projected straggle for B, P, As, and Sb in silicon. (Adapted with permission from Reference 27, copyright 1983, John Wiley and Sons).

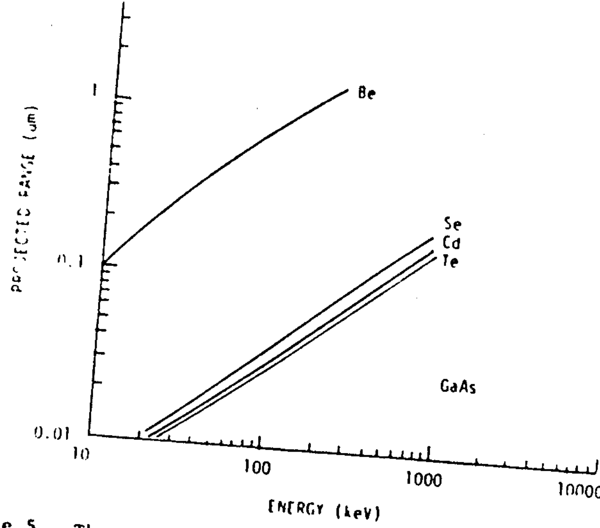


Figure 5. Theoretical calculations of the projected range of Be, Se, Cd, and Te in GaAs. (Adapted with permission from Reference 27, copyright 1983, John Wiley and Sons).

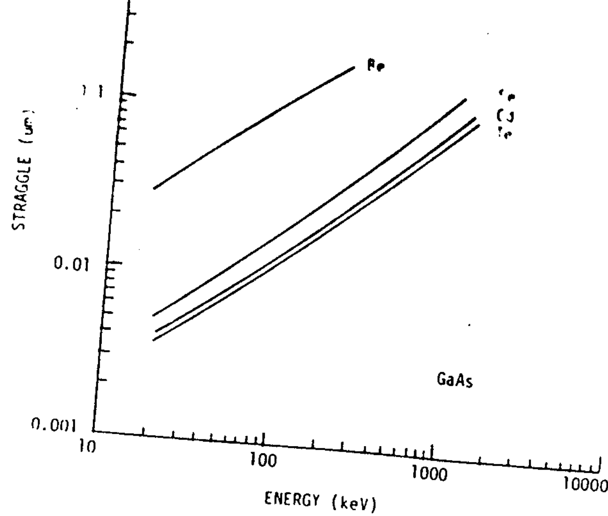


Figure 6. Theoretical calculations of the projected straggle of Be, Se, Cd, and Te in GaAs. (Adapted with permission from Reference 27, copyright 1983, John Wiley and Sons).



In the primary area of the scan, the profile expression thus becomes:

$$n(x) = N_{max} \exp\left[ - \frac{(x - \bar{R}_p)^2}{2\,\Delta\bar{R}_p^{\,2}} \right] \tag{2}$$

where $N_{max}$ is the peak of the concentration profile occurring at the point $x = \bar{R}_p$:

$$N_{max} = \frac{N_\square}{(2\pi)^{1/2}\,\Delta\bar{R}_p} \approx \frac{0.4\,N_\square}{\Delta\bar{R}_p} \tag{3}$$

$N_\square$ is defined as the ion dose in ions/cm$^2$. It is related to the total implanted charge Q in C/cm$^2$ by

$$N_\square = Q_\square / q \tag{4}$$

where q = charge on the electron.

The total implanted charge, Q, can be experimantally determined by integrating the beam current impinging on the target during the implantation time. If the beam current, I, is constant, and for implant time t:

$$Q = \frac{(I)(t)}{A} \tag{5}$$

where A is the target area scanned by the ion beam. This quantity when combined with the known energy of the accelerated ions, the theoretical values for $\bar{R}_p$ and $\Delta\bar{R}_p$ can be determined from the various curves presented. This allows the theoretical impurity concentration curves to be constructed.

An example is used to illustrate the application of the above theory. Assume that a five inch diameter silicon wafer is uniformly implanted with 80 keV boron atoms for five minutes with a constant beam current of ten microamperes. Then

$$N_\square = \frac{Q_\square}{q} = \frac{(I)(t)}{qA} \tag{6}$$

$$N_\square = \frac{10(10^{-6})(5)(60)}{q\pi\left[(5)(2.54)\right]^2/4} = 1.48 \times 10^{14} \text{ ions/cm}^2$$

For an implantation of 80 keV $B^+$ ions into a silicon target:

$\bar{R}_p$ = 2450 Å

$\Delta\bar{R}_p$ = 650Å

$$N_{max} = \frac{0.4N}{\Delta\bar{R}_p} = \frac{(0.4)(1.48 \times 10^{14})\ \text{ions/cm}^2}{650 \times 10^{-8}}$$

$$\approx 9.20 \times 10^{18}\text{cm}^{-3}$$

From this information, the theoretical concentration profile can be constructed. It should be noted that this is only a first order approximation to the actual profile. In order to more accurately fit the typical profile achieved in practice which is asymmetrical, higher spatial moments are required. These methods are discussed in much greater detail by Stone and Plunkett (26) and the references therein. The asymmetry achieved in practice has been studied by Schwettman (28) and is shown in Figure 7 from White et al (29).

## Masking Techniques

Several techniques can be used for masking the ions so as to define the area to be implanted. Usually for microelectronics a contact mask is required. Typical masks are silicon dioxide ($SiO_2$), silicon nitride ($Si_3N_4$), photoresist, or metal films. The basic requirements for a mask include:

(1) Must be compatible with the photolithographic techniques.
(2) Pattern definition should be sharp.
(3) Should have an excellent stopping power.
(4) Should not contaminate the wafer, and should be easily removable.

The minimum thickness required for various materials to stop a prescribed percentage of the ions can be estimated by the transmission coefficient, T, given by (26):

$$T = \frac{1}{2}\,\text{erfc}\left[\frac{d - \bar{R}_p}{(2)^{1/2}\Delta\bar{R}_p}\right] \qquad (7)$$

where d is the mask thickness.

For large arguments, the complementary error function can be approximated by

$$T \approx \exp(-a^2)/\,2(\pi a)^{1/2} \quad \text{where } a \text{ is given by:} \qquad (8)$$

$$a = \frac{d - \bar{R}_p}{(2)^{1/2}\,\Delta\bar{R}_p} \qquad (9)$$

To stop 99.99% of the incident ions, $T = 10^{-4}$, yielding

$a = 2.8$. Hence

$$d_{min} = \bar{R}_p + 3.96\,\Delta\bar{R}_p \qquad (10)$$

The minimum thickness for various masking materials are shown in Figures 8, 9, and 10.



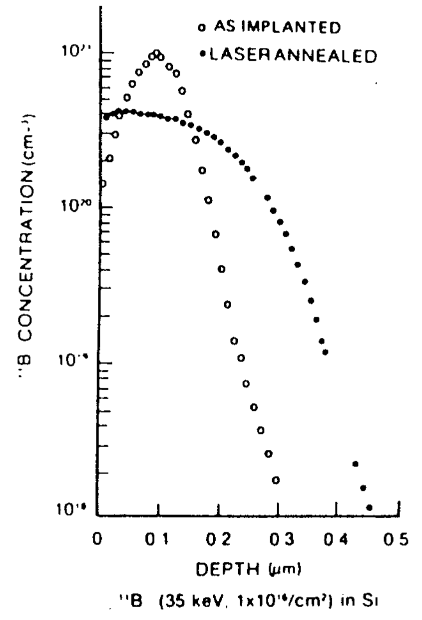


Figure 7. Experimental profile of boron implanted in silicon showing the as-implanted profile and the profile after laser annealing. (Reproduced with permission from Reference 29, copyright 1978, American Institute of Physics).

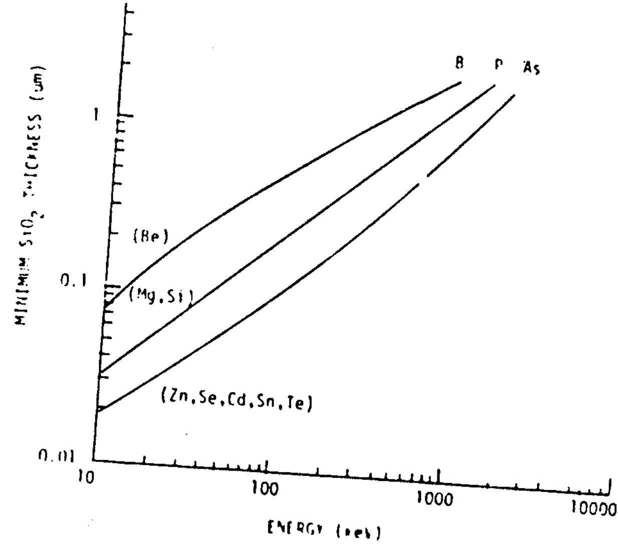


Figure 8. Calculated minimum thickness of $SiO_2$ for masking B, P, and As at various implantation energies. (Adapted with permission from Reference 27, copyright 1983, John Wiley and Sons).

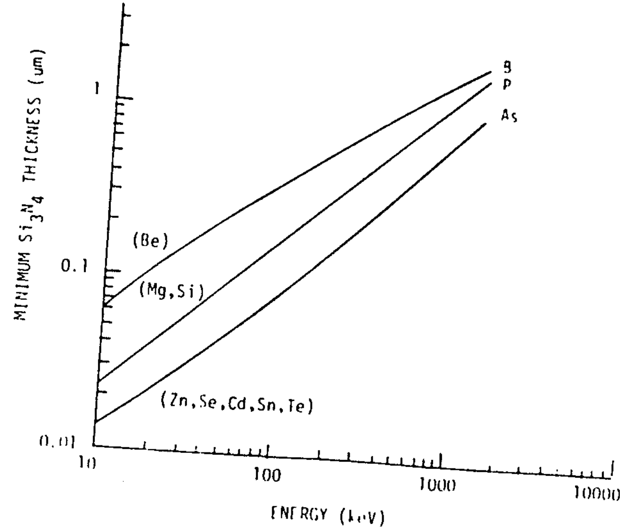


Figure 9. Calculated minimum thickness of $Si_3N_4$ for masking B, P, and As for various host materials. (Adapted with permission from Reference 27, copyright 1983, John Wiley and Sons).



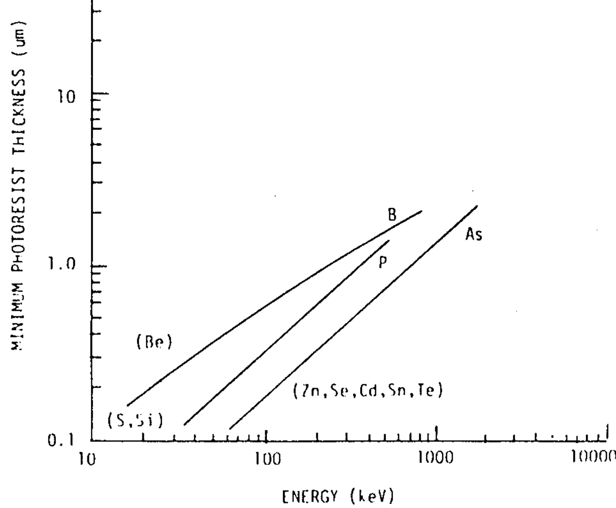


Figure 10. Calculated minimum thickness of photoresist for masking B, P, and As for various host materials. (Adapted with permission from Reference 27, copyright 1983, John Wiley and Sons).

Annealing for Electrical Activation

The basic range statistics will provide reasonable predictions of the unannealed concentration profile. Electrical activation is necessary to stabilize and ensure that the ions occupy electrically active sites. There are presently several types of anneal used for ion-implanted materials, but they can be grouped into two broad categories: 1) Thermal anneal and 2) laser anneal.

Thermal Anneal. Ion-implanted wafers should be annealed at the lowest temperature possible in order not to diffuse the impurities further into the wafer. At low implanted doses ($10^{11}$ - $10^{12}$ $cm^{-2}$) the electrical activation process can occur at temperatures as low as 260 degrees C in silicon whereas for higher doses ($10^{13}$ - $10^{14}$ $cm^{-2}$) 570 degrees C may be required. For higher doses ($10^{15}$ $cm^{-2}$) higher temperatures around 900 degrees C will be required for electrical activation (26). Most anneals are for 30 minutes in a non-oxidizing ambient. Reference 26 may be consulted for more details of the thermal anneal.

Laser Anneal. A technique for laser annealing has received considerable attention in recent years. This technique has several advantages over thermal annealing. Only the surface layer is heated sufficiently to anneal a shallow layer implant, so the substrate is unaffected. The heating is also selective, allowing small areas to be annealed without disturbing other regions. Figures 11, 12, and 13 show typical examples of as-implanted and laser annealed implants (29). The anneals were achieved by using a pulsed ruby laser with an energy density of 1.65 $J/cm^2$. Complete electrical activation was achieved.

Annealing in Gallium Arsenide. Gallium arsenide has a greater variety of defect interactions than silicon. Also, most gallium arsenide devices are based on majority carrier transport. This decreases the importance of the minority carrier lifetime. Therefore carrier activation is the primary purpose of the annealing process.

As-implanted GaAs has no carrier activation, as a rule. Higher temperatures are required to anneal GaAs material than silicon. Usually not all carriers are activated even at 900 degrees C. Therefore the annealing of GaAs presents greater problems than silicon. Moreover, often there is out-diffusion and boundary movement during anneal, as well as changes in the doping profile.

Often, GaAs is annealed by using a capping layer during the anneal. The implant is sometimes made through this cap. The cap helps to minimize out-diffusion during the anneal. Silicon nitride and aluminum oxide are typical capping materials. Temperatures as high as 1100 degrees C have been used for annealing GaAs.

Advances in Device Fabrication by Ion Implantation

The emergence of ion implantation as a primary fabrication process for a wide variety of devices has occurred at a rapid pace in recent years. The attributes of precise dopant control, low temper-



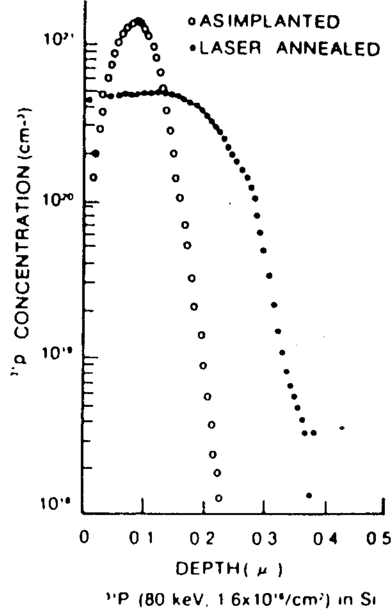


Figure 11. Experimental impurity profile of phosphorus implanted in silicon showing the as-implanted profile and the profile after annealing. (Reproduced with permission from Reference 29, copyright 1978, American Institute of Physics.)

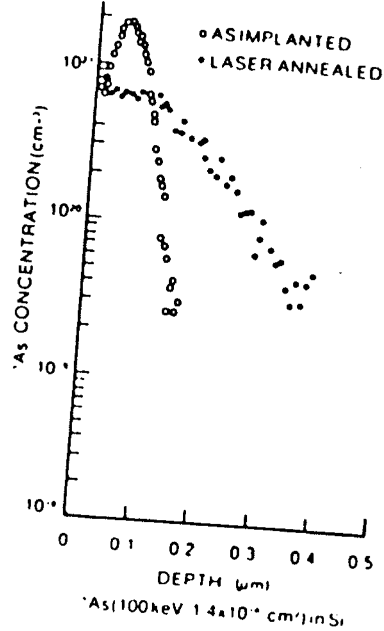


Figure 12. Experimental impurity profile of arsenic implanted in silicon showing the as-implanted profile and the profile after laser annealing. (Reproduced with permission from Reference 29, copyright 1978, American Institute of Physics.)



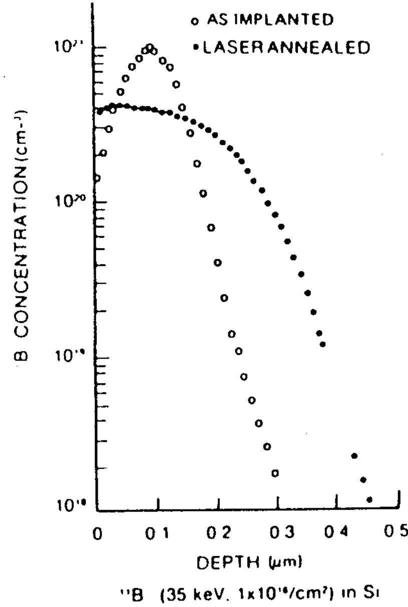


Figure 13. Experimental impurity profile of boron implanted in silicon showing the as-implanted profile and the profile after laser annealing. (Reproduced with permission from Reference 29, copyright 1978, American Institute of Physics.)

a...e, and uniformity of impurity concentration has assured its place in the development of new and improved devices. With the advent of laser and thermal pulse annealing, some of the traditional disadvantages of material damage have been minimized.

Several of the present applications of ion implantation to solid state devices are presented in Table I. The tremendous volume of literature prohibits detailed discussion of each application. However, a brief discussion of various applications is presented in the following sections.

Table I. Summary of Ion Implantation Applications in Device Fabrication

| Silicon Devices | Applications of Ion Implantation |
|---|---|
| MOS transistor | Ion implantation is used for threshold voltage adjustment. Can also be used for self-alignment with practically no gate overlap capacitance; decouples parasitic capacitances. Can be used to obtain small channel lengths (30). |
| CMOS transistor | Ion implantation provides threshold adjustment and improves the switching speed of the device. Uniformity and reproducibility of the p-channel is possible; can radiation harden the device (31,32). |
| Complementary DMOS transistor | Used as a pre-deposition step of the diffusion process. Provides superior delay time (33-35). |
| ISOMNOSFET | Implantation helps to overcome parasitic capacitance effects by better alignment (36). |
| Power FET | High energy boron implantation can be used to form highly doped buried layers for vertical channel FETs (37). |
| Subvolt JFETs | Double implanted subvolt JFETs having supply voltages at 1.5V or lower are possible with ion implantation (38). |
| Bipolar transistor | Ion implantation allows closely controlled doping profiles and eliminates parasitic devices by better lateral registration. Also can increase cut-off frequency by shallow emitter and base profiles, increasing speed and lowering the noise of the device (39-41). |
| Integrated injection logic | Shaping of the extrinsic and intrinsic base profiles by ion implantation and by closely |

Continued on next page.



Table I. Continued

| Silicon Devices | Applications of Ion Implantation |
|---|---|
| Integrated injection logic (con'd) | controlled doping density and depth improves the power-delay product and the inverse gain of the vertical npn transistors (42). |
| P-n diode | Implantation can be used to create very abrupt profiles and to closely control the depth and uniformity of the junction (26). |
| PIN diode | Ion implantation is used to fabricate the shallow high density $p^+$ region (26). |
| Avalanche photodiode | Ion implantation improves yield and signal to noise ratio. Also provides larger minority carrier lifetimes (26). |
| IMPATT diode | Implantation produces reproducible and narrow base regions for high frequency operation (26). |
| Solar cell | By the implantation process, solar cells can be made in high resistivity p-silicon by implanting phosphorus to produce shallow $n^+$ or p-layers. More favorable bulk recombination rates of minority carriers in the p-silicon causes higher collection efficiency (43-45). |
| Varactor diode | By ion implantation, the slope of the capacitance versus applied reverse voltage can be tailored by implanting phosphorus impurity profiles below the Schottky-barrier (46). |
| Schottky-barrier diode | Ion implantation is used to control the barrier height. For the PtSi Schottky-barrier diode, the aluminum-Si barrier height can be modified, the peak of which is located in the immediate vicinity of the metal-Si interface (47). |
| CCDs | The asymmetry necessary for directionality in the transfer of charge can be achieved by implanting packets of increased doping concentration near one edge of each metalization line, making the implanted region more repulsive to minority carriers at the interface than the unimplanted region. Creates a high-low junction effect (26). |

Continued on next page.

Table I. Continued

| Silicon Devices | Applications of Ion Implantation |
|---|---|
| Resistors | Ion implantation produces accurate high ohmic resistors on the order of a megohm by controlling the implant fluence and the anneal temperature (26). |
| HVSOS/MOS | Implantation provides compatibility with CMOS processing and provides low leakage, good gain, low threshold, and high breakdown (26). |

| Compound Semiconductor Devices | Applications of Ion Implantation |
|---|---|
| GaAs MESFETs | Ion implantation process creates low noise, fast devices suitable for microwave or high speed logic devices, with high gain (48-51). |
| InP MESFETs | These devices can be fabricated with even lower noise and higher gain than in GaAs by ion implantation (52). |
| GaAs MMICs | Monolithic microwave integrated circuits have been fabricated using ion implantation. This renders feasible the fabrication of monolithic phased array radars. These circuits incorporate active devices, RF circuitry, and bypass capacitors (53-54). |
| GaAs Complimentary JFETs | By ion implantation, a GaAs enhancement mode JFET has been developed in parallel with the GaAs Schottky-barrier FET or MESFET. It is useful in FET logic DCFL). Creates an ultra low power device with applications to the static RAM (55). |
| InP FETs | Ion implantation has been successfully applied to fabricate FETs on semi-insulating InP substrate. In FETs with a noise figure as low as 3.5 dB at 12 GHz have been fabricated (52). |
| GaAs Hall Devices | Implantation has been used to fabricate highly linear GaAs Hall devices. Linearity error is better than ± 0.03% (56). |



The extent of the applications of ion implantation to the fabrication of silicon devices prohibits an in-depth treatment of each application. A more complete discussion of these applications can be found in review form in Reference 26 and the references therein. This presentation therefore deals primarily with the fundamentals of ion implantation and the methodology of applying some of these fundamentals to advanced device technology.

Field Effect Transistor Applications. Among the advantages of ion implantation in field effect device fabrication are:

(1) Threshold adjustment for compatibility with TTL logic.
(2) Depletion mode/enhancement mode fabrication.
(3) Improved frequency response.
(4) Low temperature and simple process.
(5) Self-alignment of MOS divices.
(6) Channel stop fabrication.

Ion implantation can be used for gate self-alignment in MOS devices. Using boron implantation at about 80 keV, the aluminum gate or thick oxide will mask the ion beam. But when a thin oxide (approximately 1200 Å) is positioned over the remaining part of the silicon surface, the beam will penetrate the thin oxide, and be deposited in the silicon surface at the $Si-SiO_2$ interface, extending the source and drain to the gate boundary. The gate field plate has masked the ions from the gate region. After implantation of about $10^{14}$ $ions/cm^2$, the devices are annealed at about 400 to 500 degrees C for about 30 minutes. Figure 14 shows a MOSFET device requiring two implantations, the n-implantation forms a self-aligned source and drain region. The p-implantation permits a short channel length with the high resistivity substrate material required to reduce capacitances.

Use of this self-alignment process provides the advantages of essentially no overlap capacitance, and improves the speed by a factor of 30 to 40%.

Ion implantation through an oxide can also be used to increase the threshold voltage outside the channel region (27). Figure 15 illustrates how a channel stopper of this type can be fabricated by a single unmasked high energy implant. To complete this step, a 200-300 keV boron implant is used if the device is an n-channel MOSFET. Since this implantation penetrates deeply under the thin gate oxide, it does not affect the threshold voltage. However, the regions of thick oxide receive a shallow implant in the p-type field regions. It therefore increases the threshold voltage necessary to create parasitic action.

Ion implantation when used for channel doping has the following advantages:

(1) The threshold voltage can be adjusted to accommodate direct interfacing with TTL circuitry.

(2) A high ratio of field threshold-to-device threshold is obtained.

(3) Depletion mode load/enhancement mode driver circuitry are achieved on one chip.

This results in higher circuit density, improvement in the speed/power product, and the device can operate from a single 5 volt supply. In this process, ion implantation is used to dope the MOSFET channel with boron at an energy of about 50 keV. The range of these ions are such that they penetrate the 1200 Å gate oxide

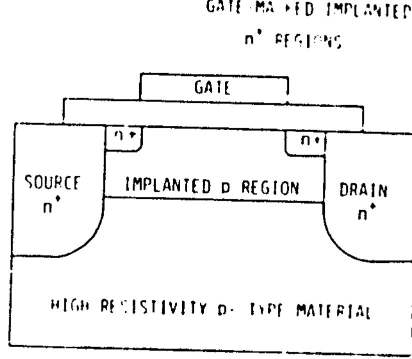


Figure 14. Typical MOSFET requiring two ion implantations.

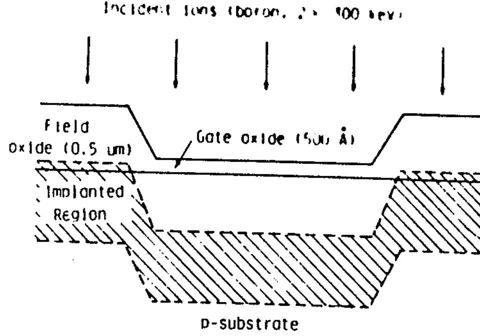


Figure 15. Ion implantation used for channel stopping. (Adapted with permission from Reference 27, copyright 1983, John Wiley and Sons).



and stop in the silicon surface region. Because of ion straggling in the range, a layer of approximately 0.2 micrometers is obtained at the silicon surface. The device is then annealed. A PMOS example is presented below:

If $6 \times 10^{16}$ $cm^{-3}$ boron atoms are implanted in the gate region of the p-channel MOSFET fabricated on <111> oriented n-type material with $N_D = 10^{15}$ $cm^{-3}$, the compensated results yields:

$$p = N_A - N_D = 6 \times 10^{16} - 1 \times 10^{15} = 5.9 \times 10^{16} \text{ cm}^{-3}$$

The channel will be p-type. If the channel is assumed to be uniformly implanted to a depth of 0.2 micrometer, then only $1.18 \times 10^{12}$ boron atoms/$cm^2$ are implanted. For approximately $10^{12}/cm^2$ boron atoms implanted, and if a beam density of $10^{-2}$ microamperes/$cm^2$ of singly charged boron ions is used, then:

$$\text{Implanted atoms/cm}^2 = \frac{\text{(beam current density)}}{q} \times \text{time}$$

$$10^{12}/\text{cm}^2 = \frac{10^{-8} \text{ A/cm}^2}{1.6 \times 10^{-19}\text{C}} \times t$$

Solving for t: t = 22 seconds.

The implantation time required to provide the dose indicated is then 22 seconds.

In CMOS (complementary metal-oxide-semiconductor) technology, the p-channel is fabricated by ion implantation. Using this technique, 5% control in the doping is possible and the threshold control is improved.

The ISOMNOSFET has two features which are not in the conventional MNOSFET. It has a stepped oxide in the channel region, and an ion implanted region adjacent to the channel. By using a stepped oxide with two oxide thicknesses in the channel, two constant threshold thick-oxide FETs in series with the thin oxide variable threshold device ensures that the composite device maintains operation in the enhancement mode in both the high and low threshold states.

Ion implantation is used in the fabrication of low-barrier PtSi Schottky-barrier diodes. An ion-implanted, shallow $n^+$ layer has been used by Bindell et. al. (57) to lower the barrier height of PtSi-n-Si Schottky diodes. Barrier height reductions of up to 200 mV have been achieved. This implant increases the electric field at the surface, thus lowering the effective barrier height through an enhanced Schottky lowering effect (57).

Ion implantation has also been used to increase the barrier height of metal-semiconductor Schottky-barrier diodes (46). This is accomplished by implanting low energy ions of opposite conductivity type into the semiconductor surface. The implanted ions change the field and potential in the surface region and reduce the diode current. Figure 16 shows the variation of current density versus forward voltage for various values of ion implantation dose (58).

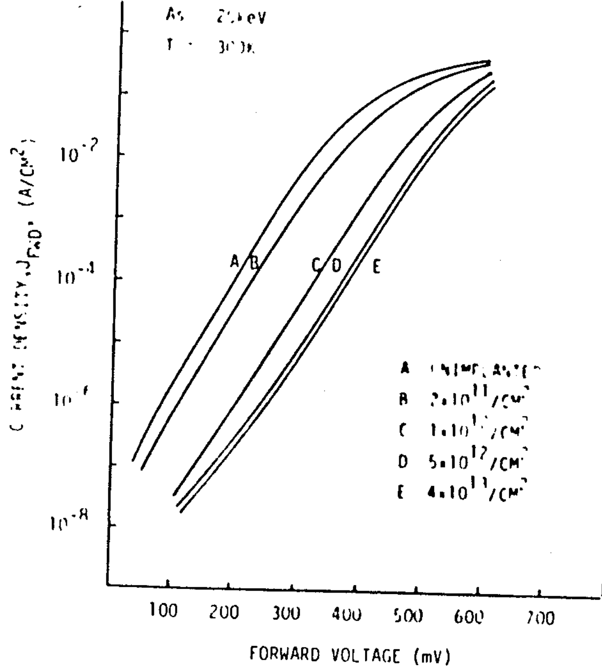


Figure 16. Calculated diode current density versus forward voltage curves for various values of ion implantation dose. (Adapted from Reference 43.)



In the fabrication of hyperabrupt diodes such as varactors, the flexibility in doping profiles that can be produced by ion implantation allows a wide range of capacitance-voltage characteristics to be designed.

Figure 17 shows the impurity profile of a hyperabrupt Schottky diode. In varactor diodes, ion implantation can be used to tailor the slone of the capacitance versus applied reverse voltage by implanting phosphorus impurity profiles below the Schottky barrier.

Bipolar Transistors and Integrated Injection Logic. The dosage control and profile shaping attributes of ion implantation make it ideal for the fabrication of high frequency, high gain, low noise transistors. Archer (39) in his work separately implanted the inactive and active base regions in 8 GHz transistors. The excellent results were attributable to the close dose control of the active base Gummel number (26). Stone and Plunkett (26) have also found that this technique significantly improves the inverse gain of bipolar transistors when properly carried out. Arsenic emitters are also preferred for low loise and abrupt profiles, thus improving emitter efficiency. Other researchers have used ion implantation in the fabrication of super-gain transistors and high performance transistors with arsenic implanted polysil emitters (40).

Ion implantation is well suited for the design of bipolar structures used in injection logic. Among the attributes of ion implantation for these are 1) ability to fabricate shallow devices thus improving the speed and gain and tailoring the impurity concentration profiles. Separate implantations for the inactive and the active base layers are usually desirable.

It should be remembered that in integrated injection logic, the vertical npn transistor must be operated in the inverse mode. Figure 18 shows the top view of an $I^2L$ unit cell, and Figure 19 shows the cross sectional view. The impurity concentration profile of a typical $n^+pnn^+$ transistor is shown in Figure 20. Figure 21 shows superimposed on the initial profile, an LEC profile which has been modified to provide an aiding field in the intrinsic base region, plus a low doped region for the inverted collector. This reshaping of the impurity profile has been found to improve the inverse gain and switching speed of the integrated injection logic unit cell (41).

For the most part, one may assume that in the inverse mode the opposite to those forward-mode attributes is true. A larger portion of the field is retarding than aiding, and the overall effect is retarding. This increases the base transit time of the inverse transistor, thus lowering the $f_T$ and switching speed.

It is obvious therefore that if the base profile could be reshaped or tailored to some optimum shape, the switching speed of the transistor would be improved. Several researchers have studied improved shapes of the base profile in search of an optimum. It turns out that optimum shapes for some attributes of the transistor do not optimize others. Among the shapes that have been studied are 1) Gaussian, 2) Complementary error function, 3) Exponential, 4) Parabolic, and 5) Segmented.

The exponential distribution has been shown to be the best of the group for minimum transit time (41). The segmented profile,

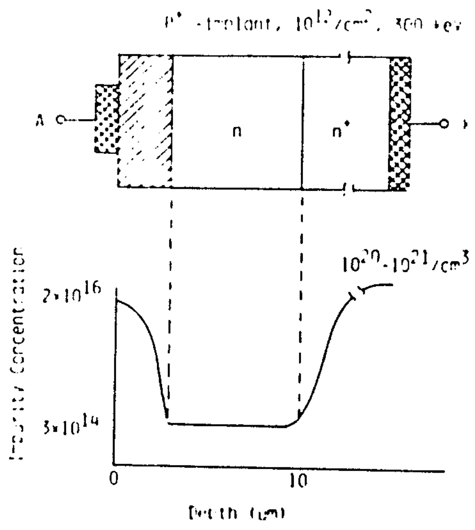


Figure 17. Hyperabrupt Schottky diode.

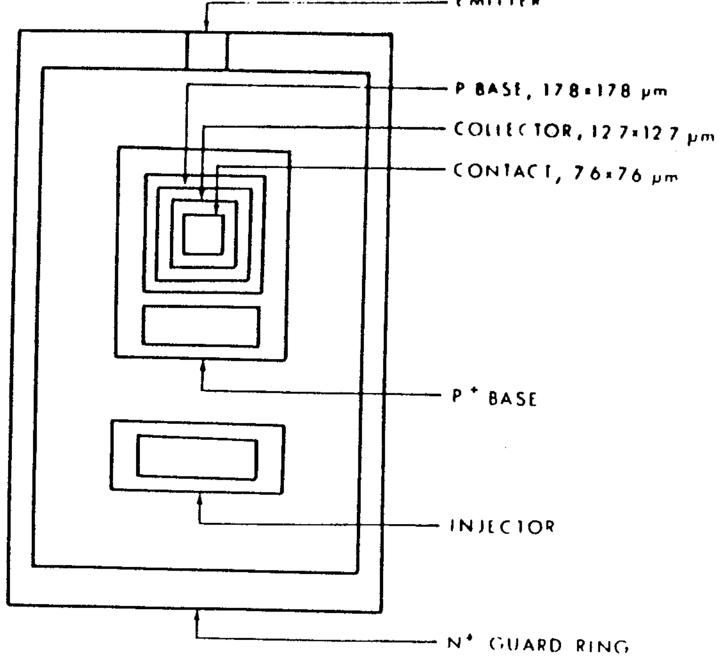


Figure 18. Top view of integrated injection logic unit cell. (Reproduced from Reference 41).



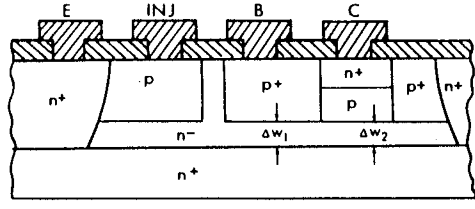


Figure 19. Cross section view of integrated injection logic chip. (Reproduced from Reference 41).

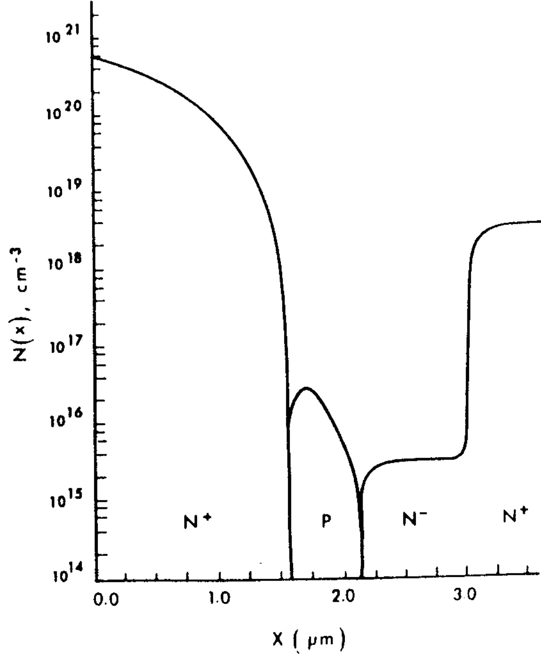


Figure 20. Impurity concentration profile of a bipolar transistor fabricated by diffusion. (Reproduced from Reference 41).

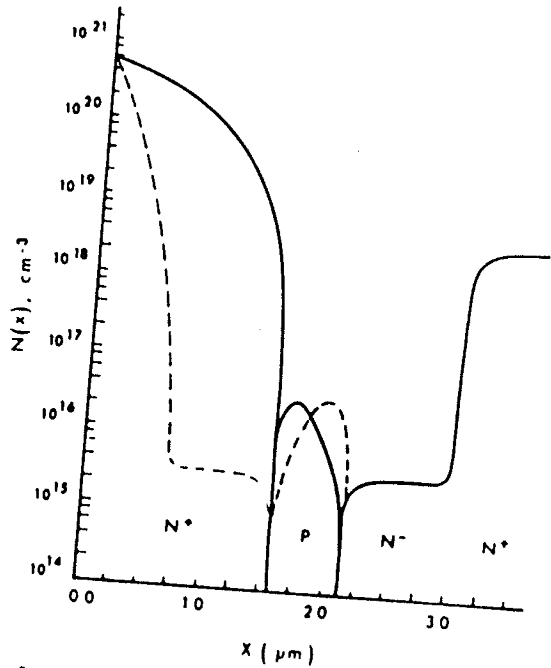


Figure 21. Impurity concentration profile showing possible profile shaping by ion implantation for improved operation in the inverse mode. (Reproduced from Reference 41).



having small widths of retarding field followed by a large region of aiding field yields a larger figure of merit for switching transistors (41). The figure of merit used by Maheshwari and Ramanan is (59):

$$F = \frac{1}{t_b r_b C_c} \qquad (11)$$

where $t_b$ is the base transit time, $r_b$ is the base spreading resistance, and $C_c$ is the base-to-collector capacitance. They found that a profile which has a retarding field over a portion of the base and an aiding field over the other improves the figure of merit compared with the exponential distribution. Ion implantation could be used to shape this profile. By using ion implantation, the base Gummel number can be precisely controlled since the use of current integration for the dose measurement allows the base impurities to literally be counted. Further discussion of the device parameter optimization by ion implantation is treated by Stone and Plunkett in Reference 26.

Experimental measurement of the doping profiles for ion implantation can be performed by anodization and stripping for high accuracy as given in Reference 41. Figure 22 shows the set-up. One excellent chemical for the anodization solution is a mixture of tetrahydrofurfuryl alcohol (THF) and potassium nitrite ($KNO_2$). The proper mixture is 2.8 g of $KNO_2$ per 100 ml of THF. The solution should be irradiated during the process with a tungsten-halogen lamp to accelerate the anodization process. A typical constant current used is about 10-15 mA/cm$^2$. The oxide thickness is proportional to the final forming voltage, and for the conditions described is about 4 Å/volt (41). Figure 23 shows a typical measured and plotted profile. An algorithm for processing the data is given in Reference 41.

Ion Implanted Resistors. If a substrate is doped with a layer of impurities opposite to that of the background doping, the resistivity is given by the total number, $N_s$, of the mobile carriers/cm$^2$ and the mobility:

$$R_s = \frac{1}{q\mu N_s} \qquad (12)$$

Ion implantation can provide accurate control over $N_s$ and reduce the mobility (26).

### Advances in Compound Semiconductor Ion-implanted Devices

Many of the device technologies which are common in silicon, such as MOS technology, have yet to be developed in the compound semiconductors. Researchers are presently pursuing these areas. A variety of problems are presented in the development of some of these technologies. Heavy doping necessary for certain areas of the devices is difficult to achieve by simple processes in gallium arsenide. In spite of these shortcomings, there are several areas in which ion implantation has already been successfully used. With

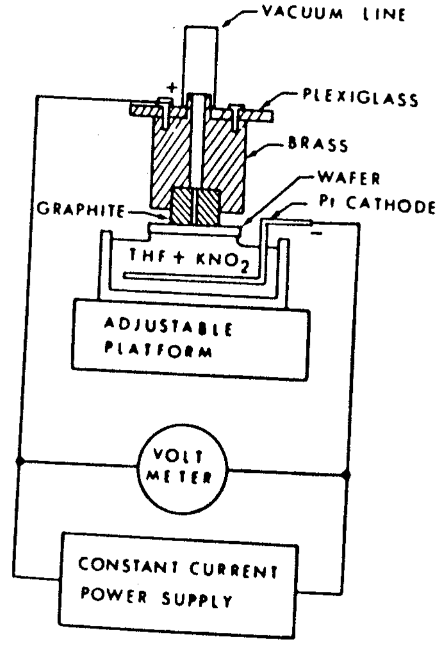


Figure 22. Experimental laboratory apparatus for the anodization and stripping of silicon. (Reproduced from Reference 41).



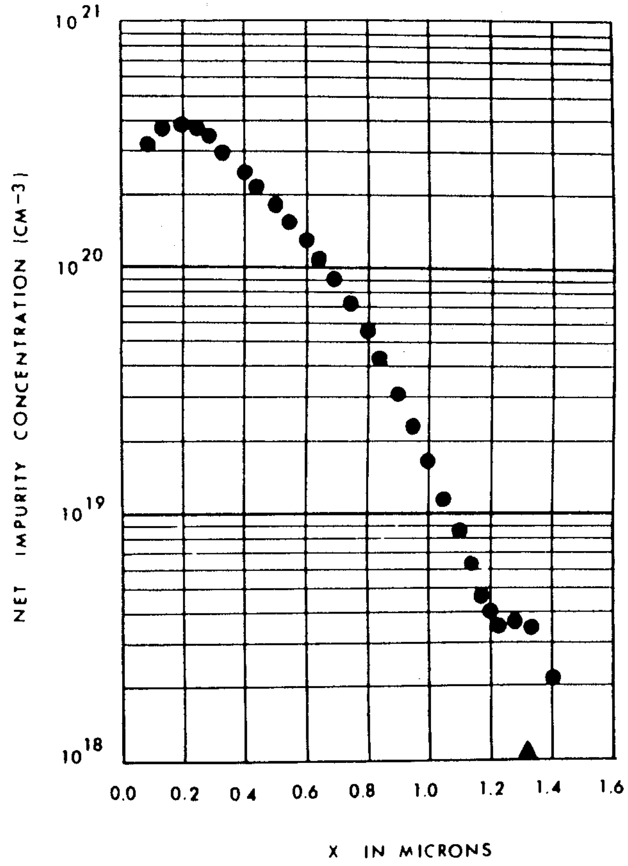


Figure 23. Results of impurity profile measurement by anodization and stripping technique. (Reproduced from Reference 41).

increasing needs for development in these areas of Gigabit logic and microwave power devices, compound semiconductors such as gallium arsenide are excellent candidates. Gallium arsenide shows significant promise because of its higher mobility and other attributes. A brief discussion of several applications of ion implantation in gallium arsenide devices are outlined here. Golio (60) et. al. have studied the potential of a number of compound semiconductors for low noise microwave MESFET applications. The industry is making continuous advances in the development of GaAs field-effect transistors for microwave applications. These devices have been shown to exhibit excellent noise performance through the K-band. Moreover, as the requirements for VLSI memory and logic become more stringent, and greater demands are placed upon the attributes of speed and low power consumption, MESFETs look more and more attractive. Golio's study included models of GaAs, InP, GaInAs, InPAs, and other devices. Comparison of a $Ga_{0.5}In_{0.5}As_{0.96}Sb_{0.04}$ device to a conventional gallium arsenide device indicated that a decrease in the minimum noise figure by a factor of two is possible. Some of the other compound semiconductor devices also showed improvement in the noise figure.

Sleger et al. (52) have reported the development of ion-implanted one micron gate length InPFETs with noise figures as low as 3.5 dB at 12 GHz. When compared with similar GaAs devices, superior gains at microwave frequencies over that of GaAs was demonstrated. Further improvement in profile optimization of the implanted area appears feasible as a means of further reduction in the noise figure.

The development of monolithic microwave amplifiers formed by ion implantation into LEC gallium substrates have been reported by Driver et al. (54). These monolithic power integrated circuits on semi-insulating gallium arsenide are expected to provide improved bandwidth over hybrid microwave circuits because of improved matching environments and the reduction of parasitic inductances due to wire bonds. As this technology is evolved, it is entirely feasible that phased array radars could be fabricated with these monolithic chips. Driver has built one and two stage monolithic GaAs power amplifiers operating from 5 to 10 GHz using standard photolithographic masking with the addition of a chlorobenzene process to help the metal liftoff. Powers of 28 dBm across a bandwidth of 5.7 to 11 GHz with 6 dB gain have been achieved. Gupta et al. (51) have also reported process improvements in MESFET GaAs monolithic microwave circuits. Gupta (52) in a later paper has detailed an ion-implantation fabrication process for fabricating GaAs monolithic microwave integtated circuits (MMICs), incorporating active devices, RF circuitry, and bypass capacitors.

Feng et al. (49) have reported the fabrication of GaAs MESFETs by ion implantation into MOCVD (metal organic chemical vapor deposition) buffer layers. Recently, metal organic chemical vapor deposition has been used for the fabrication of the channel layers in GaAs FETs (49). Feng reports a reporducible process using ion-implanted MOCVD buffer layers for low noise MESFETs. The buffer layers were grown by the MOCVD technique on <100> Cr-doped semi-insulating GaAs substrates. After degreasing, the substrates were etched in HCL for one minute and in a solution of 5:1:1 $H_2SO_4$: $H_2O_2$: $H_2O$ at 40 degrees C for two minutes; then they were rinsed in deionized water for 20 minutes. After blowing dry in dry $N_2$ and loaded into the MOCVD chamber, the growth was done at a temperature of 650 degrees C at atmospheric pressure. The buffer layer is approximately 2 microns thick with net carrier concentration of $3 \times 10^{15} cm^{-3}$ and a mobility of 6500 $cm^2$/V-sec.



The channel layer was formed by direct ion implantation with a Si ion dose of $6.5 \times 10^{12} cm^{-2}$ at 100 keV. Annealing at 850 degrees C in $H_2$-$As_4$ was performed. Results of the best device showed a noise figure of 1.46 dB with a gain of 10.2 dB at 12 GHz. The results indicate that a high degree of microwave uniformity can be achieved by ion implantation into MOCVD buffer layers.

Zuleeg et al. (55) have reported the fabrication of a double-implanted GaAs complementary JFET. The GaAs enhancement mode JFET was developed in parallel with the GaAs Schottky-barrier FET or MESFET. It is useful for direct coupled FET logic (DCFL). Reduction in the required power level by an order of magnitude (from about 100 microwatt/gate) is possible by using complementary n-channel and p-channel enhancement mode JFETs. Zuleeg has reported a double-implantation of n-channel and p-channel enhancement GaAs FET and its application to an ultra-low power static RAM. The reader is referred to Zuleeg's paper for the process steps.

Heterojunction bipolar transistors (HBTs) are currently receiving increased attention by researchers for high speed applications. To meet these requirements, transistors must be fabricated with smaller emitter widths and better contacts to the p-type base region. Ion implantation is presently being used to accomplish these requirements. The high temperature annealing required presents a problem, however. Asbeck et al. (61) have reported a thermal annealing (pulsed) technique for annealing the ion implanted devices. Application of the technique was made to the fabrication of Be-implanted MBE (molecular beam epitaxy) grown GaAlAs/GaAs heterojunction bipolar transistors. The thermal annealing was shown to compare well with the furnace annealing (non-pulsed) without the occurrence of impurity diffusion.

## Systems for Ion Implantation

Most of the ion implantation systems have the same basic elements, only differing in the details and perhaps level of automation. A schematic diagram of a typical ion implantation system is shown in Figure 24.

For the purpose of this discussion it will be assumed that the Nielson source is used. It consists of a cylindrical arrangement of a tungsten helical cathode , a cylindrical anode of graphite and a magnet coil. Solid materials can be vaporized in an oven with two types of crucibles where temperatures ranging from 170 to 900 degrees C can be covered. The lifetime of a source is about 30 hours. Typical source materials are $BF_3$, phosphorus ($PF_3$), and $AsF_3$.

Typical ion sources work on the basic principle that a confined electric discharge or arc is partially or completely sustained by the gas or vapor of the material that is being ionized. The hot cathode source consists of a hot emitting electrons (usually

a filament) and an anode. The presence of a small amount of gas whose ionization potential is less than the potential between the electrodes will cause the primary electrons to produce positive ions. A diagram of a Nielson source is shown in Figure 25. For further discussion of ion sources the reader is directed to Reference 62.

The beam is then focused, pre-accelerated, and passed through a mass analysis stage. After fucusing, the beam is accelerated to its final energy by a linear accelerator. The beam is again focused by a doublet quadrupole before entering the x-y scanning system. Electrostatic scanning in the x and y directions is provided. A trap is provided for uncharged, neutral species while the selected ions are deflected to the target. A vacuum of below $10^{-6}$ Torr is necessary for the system.

A typical target chamber is shown in Figure 26. The chamber can be a carousel type which rotates to a series of wafers for implantation.

## Appendix

### Chemical Processing for Ion-implanted Integrated Circuits

Detailed cleaning and processing steps are often not published by the industry. For university researchers and students, however, this often becomes a problem. Often they are forced to consume an inordinate amount of time developing a routine process for cleaning and basic processing. The author faced such a delimma a few years ago while a doctoral student, and in order to ease the burden of some poor graduate student, the following procedure has been found acceptable by the author for certain photolithographic operations. It is hoped that this may save some time for the student if he does not have a workable procedure.

Initial Wafer Cleanup. The following procedure should be done in a class 100 clean room:

1. 10% HF in DI water solution at 25 deg. C for 6 min.
2. Cascade rinse in DI water for 6 min.
3. Tetrachlorethylene at 80 deg. C for 6 min.
4. Cascade rinse in DI water for 6 min.
5. Ammonium Hydroxide mixture at 80 deg. C for 6 min.
6. Cascade rinse in DI water at 25 deg. C for 15 min.
7. HCL mixture at 25 deg. C for 6 min.
8. Cascade rinse in DI water at 25 deg. C for 15 min.
9. Blow dry with dry nitrogen.
10. Bake in process clean oven at 135 deg. C for 10 min.
11. The wafer should be used within 20 minutes after the cleanup.

Predeposition Cleanup. The following procedure should be done in a class 100 clean room:

1. Agitate in Nitric acid at 90 deg. C for 6 min.
2. Cascade rinse in DI water for 10 min.
3. Slowly agitate in 10% HF for about 5 sec. depending on doping level of prior steps.
4. Rinse immediately in DI water for 15 min.
5. Cascade rinse in DI water for 15 min.
6. Blow dry with dry nitrogen.



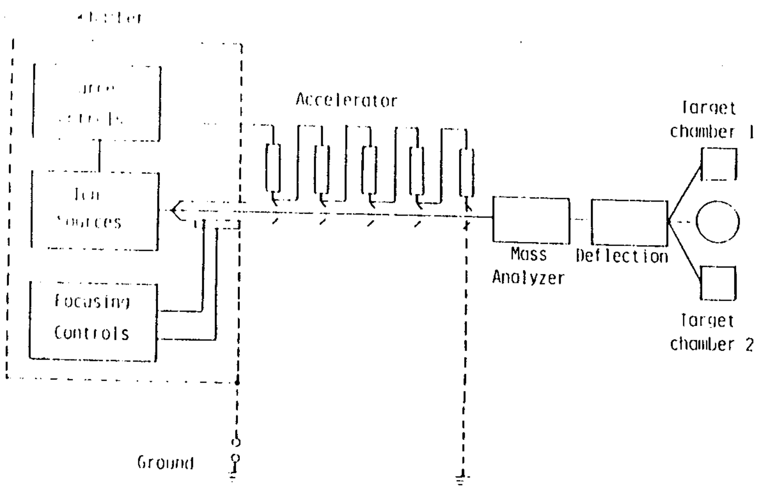


Figure 24. Block diagram of an ion implantation system.

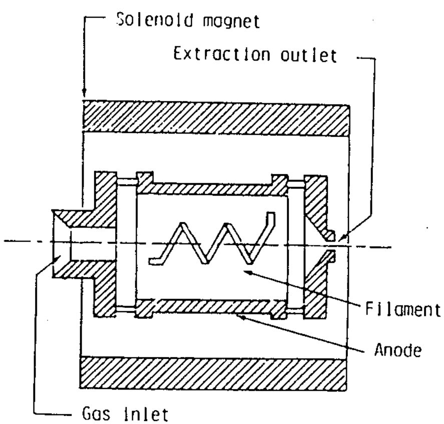


Figure 25. Nielson-type source for ion implantation.

14. Plunkett, J. C.; Stone, J. L. Solid St. Tech. 1975, 18, 49.
15. Reddi, V. G. K.; Yu, A. Y. C. Solid St. Tech. 1972, 15, 35.
16. Seager, D. K.,"NTIS Report No. SC-B-71048, Supplement I", Sandia Laboratories, 1973.
17. Stephens, J., The Radio and Elect. Engr. 1972, 42, 265.
18. Stone, J. L.; Plunkett, J. C. Solid St. Tech. 1976, 19, 35.
19. Stone, J. L.; Plunkett, J. C. "Ion Implantation Processes in Silicon, Ch 2, Impurity Processes in Silicon", North Holland, Amsterdam, 1981.
20. Titov, V. V. Phys. Stat. Sol. 1978, 48, 13.
21. Lindhard, J.; Scharff, M.; Schiott, H. E. Mat. Fys. Medd. Dan. Vid. Selsk 1963, 33, 14.
22. Gibbons, J. F. Proc. IEEE. 1968, 56, 295.
23. Johnson, W. S.; Gibbons, J. F. "Projected Range Statistics in Semiconductors", Standord University, 1969.
24. Lindhard, J.; Scharff, M. Phys. Rev. 1961, 124, 128.
25. Gibbons, J. F.; Johnson, W. S.; Mylroie, S. W. "Projected Range Statistics," 2nd Ed., Dowden, Hutchinson, and Ross, 1975.
26. Stone, J. L.; Plunkett, J. C. "Ion Implantation Processes in Silicon, Ch 2 Impurity Doping Processes in Silicon", Edited by F. Y. Y. Wang, North Holland, Amsterdam, 1981.
27. Ghandhi, S. K. "VLSI Fabrication Principles", Wiley & Sons, 1983.


TK 7874 G473 1994


28. Schwettman, F. N. J. Appl. Phys. 1974, 45, 1918.
29. White, C. W.; Christie, W. H.; Appleton, B. R.; Wilson, S. R.; Pronko, P. D.; Magee, C. W. Appl. Phis Lett. 1978, 33, 662.
30. MacDougall, J. K. Electronics. 1970, 43, 86.
31. Dingwall, A. G. F.; Stricker, R. E. IEEE J. Solid St. Circ. SC-12, 1977, 344.
32. Declercq, M. J.; Laurent, T. IEEE J. Solid St. Circ. 1977, SC-11, 264.
33. Lin, H. C.; Halsor, J. L. IEEE J. Solid St. Circ. 1976, SC-11, 443.
34. Masuhara, T.; Muller, R. S. IEEE J. Solid St. Circ. 1976, SC-11, 453.
35. Troutman, R. R. IEEE Trans. Electron Dev. 1977, ED-24, 182.
36. Krick, P. J. IEEE Trans. Electron Dev. 1975, ED-22.
37. Ozawa, O.; Iwasaki, H. IEEE Trans. Electron Dev. 1978, ED-25, 56.
38. Satwinder, et. al., Solid St. Electronics. 1981, 25, 791.
39. Archer, J. A. Solid St. Electronics, 1974, 17, 387.
40. Gregg, W. M.; Saltich, J. S.; Roop, R. M.; George, W. L. IEEE J. Sol. St. Circ. 1976, SC-11, 485.
41. Plunkett, J. C. PhD Dissertation, Texas A&M University, 1978.
42. Young, R. T.; White, C. W.; Narayan, J.; Westbrook, R. D.; Wood, R. F.; Cristie, W. H. "13th Annual IEEE Photovoltaic Specialist Conf.", Washington, DC, June 5-8, 1978.
43. Kirkpatrick, A. R.; Minnucci, J. A.; Greenwald, A. C. "13th Annual IEEE Photovoltaic Specialist Conf." Washington, DC (June 5-8, 1978).
44. Pai, Y. P.; Lin, H. G. "13th Annual Photovoltaic Specialist Conf." Washington, DC (June 5-8, 1978).





45. Mulder, J. C.; Grob, J. J.; Stuck, R.; Siffert, P. "13th Annual IEEE Photovoltaic Specialist Conf." Washington, DC (June 5-8, 1978).
46. Moline, R. A.; Foxhall, G. IEEE Trans. Electron Dev. 1972, ED-12, 267.
47. Ashok, S. et al. EDL-5. 1984, 2, 48.
48. Masao, Ida, et al. Solid State Electronics. 1981, 24, 1099.
49. Feng, M.; et al. EDL-5. 1984, 1, 18.
50. Taylor, G. et al. IEEE Trans. Electron Dev. 1979, ED-26.
51. Gupta, A. K. et al. IEEE EDL. 1983, 12, 1850.
52. Sleger, K. J., et al. IEEE Trans. Electron Dev. 1981, ED-28, 1031.
53. Gupta, A., et al. IEEE Trans. Electron Dev. 1983, ED-30, 16.
54. Driver, M., et al. IEEE Trans. Electron Dev. 1981, ED-28, 191.
55. Zuleeg, R., et al. IEEE EDL. 1984, EDL-5, 21.
56. Hara, T., et al. IEEE Trans. Electron Dev. 1982, ED-29, 78.
57. Bindall, J. B., et al. IEEE Trans. Electron Dev. 1980, ED-27, 420.
58. Pai, Y. P.; Lin, H. C. Solid State Elect. 1981, 24, 929.
59. Maheshwari, L. K.; Ramann, K. V. Solid State Elect. 1976, 19, 307.
60. Golio, J. M., et al. IEEE Trans. Electron Dev. 1983, ED-30, 1844.
61. Asbeck, P. M., et al. IEEE EDL. 1983, EDL-4, 81.
62. Nielson, K. O. Nucl. Instrum. and Methods. 1957, 1, 289.


RECEIVED August 1, 1985

VLSI Handbook TK7874.V563 1985
7874.75 V573 1999

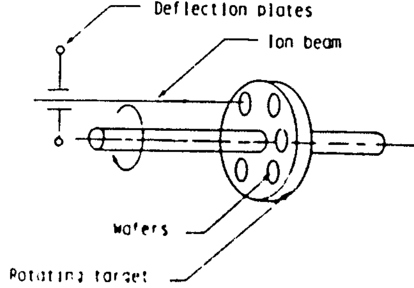


Figure 26. **Target of an ion-implantation system.**



7. Bake at 135 deg. C for 10 min.

Oxide Removal. The following procedure should be done in a class 100 clean room:
1. Use Bell 2 etchant (there is less undercutting than with HF).
2. The etch rate is approximately 750 Angstroms/min. in low doped oxides.
3. Solution preparation:
   a. 200 ml DI water
   b. 200 g. $NH_4F$ (filtered Ammonium Flouride)
   c. 45 ml HF (49%)

Aluminum Etching Procedure. The following procedure should be done in a class 100 clean room:
1. Etch at room temperature. The following mixture is satisfactory:
   a. 75% $H_3PO_4$
   b. 22% Acetic acid
   c. 3% Nitric acid
2. Agitate constantly and observe wafer to see when the slice is clear. Etch rate is approximately 1 micron per 30 minutes.

Formulas for Mixtures Used in Initial Wafer Cleanup.
1. Ammonium Hydroxide mixture: Mix 5 parts DI water, one part $NH_4OH$; heat to 80 deg. C; then add 1 part $H_2O_2$ (30% unstabilized) This is added just before using and heated back to 80 deg. C.
2. HCL Mixture: Mix 6 parts DI water, 1 part HCL; heat to 80 deg. C; add 1 part $H_2O_2$.

Literature Cited

1. Agajanian, A. H. Rad. Eff. 1974, 23, 73.
2. Brewer, G. R. IEEE Spect. 1971, 8, 23.
3. Dearnaley, G. "Ion Implantation, Annual Review of Materials Science." 1974, 4, 93.
4. Dearnaley, G.; Freeman, J. H.; Nelson, R. S.; Stephen, J. "Ion Implantation Defects in Crystalline Solids"; North Holland, Amsterdam, 1973, 8.
5. Dill, H. G.; Finnila, R. M.; Luepp, A. M.; Toombs, T. N. Solid St. Tech. 1972, 15, 27.
6. Gibbons, J. F. Proc. IEEE, 1968, 56, 295.
7. Gibbons, J. F. Proc. IEEE, 1972, 60, 1062.
8. Lee, D. H.; Mayer, J. W. Proc. IEEE, 1974, 62, 1241.
9. Mayer, J. W.; Marsh, O. J. "Ion Implantation in Semiconductors", Academic Press, New York, 1971, 1.
10. Mayer, J. W., Davies, J. A.; Eriksson, L. "Ion Implantation in Semiconductors", Academic Press, 1970.
11. Mazzio, J., "NTIS Report No. SC-B-710148", Sandia Laboratories, 1971.
12. Morgan, R.; Greenhalgh, K. R., "AERE-Bib-176", Atomic Research Establishment, Harwell, England, 1972.
13. Pickar, K. A., "Ion Implantation in Silicon--Physics, Processing, and Microelectronic Devices", Academic Press, New York, 1975, 5.